HEY! Check This Out! **Back by Popular Demand!**

"Silicon-Based Heterostructure Devices and Circuits"

ECE 6444 Fall Semester 2018

When / Where: Tues/Thurs 1:30-2:45pm, Gugg[AE] room 246
Instructor: John D. Cressler (521 TSRB, cressler@ece.gatech.edu)
Prerequisites: Modest Background in Semiconductor Devices (UG are welcome)

Course Description

Microelectronic device and circuit designers have long sought to combine the superior transport properties and design flexibility offered by bandgap engineering (as routinely practiced in compound semiconductors such as GaAs and InP), with the high yield and low cost of conventional silicon (Si) fabrication. With the introduction of epitaxial silicon-germanium (SiGe) alloys, that dream finally became a reality. The SiGe heterojunction bipolar transistor (SiGe HBT) was the first practical bandgap-engineered device to be realized in the Si material system. The first functional SiGe HBT was demonstrated in 1987, and the technology has matured rapidly, at present achieving a unity-gain cutoff frequency above 700 GHz, circuit delays below 2 picoseconds, and integration levels sufficient to realize a host of record-setting digital, analog, RF, mm-wave, and sub-mm-wave circuits. Naturally-compatible, the integration of SiGe HBTs with best-of-breed Si CMOS to form a SiGe HBT BiCMOS technology is an obvious fit for addressing emerging performance-constrained, highly integrated systems, and is currently being pursued globally in the commercial and defense sectors.

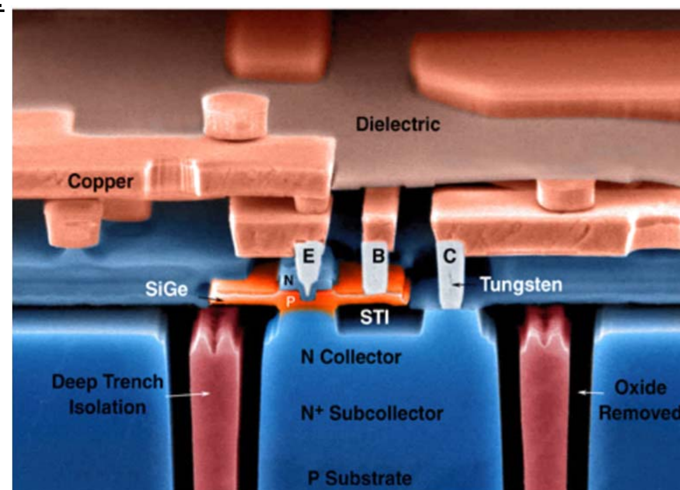
"Silicon-Based Heterostructure Devices and Circuits" presents an in-depth examination of this exciting field. The course will begin with some background and motivation, and then a discussion of SiGe strained-layer epitaxy. This will be followed by a detailed examination of the SiGe HBT, including fabrication, profile design, fundamental physics, static and dynamic properties, and a host of other issues related to profile optimization. We then address circuit-level design with SiGe HBTs, including noise, linearity, and compact modeling issues. We conclude with an overview of other emerging device types which are enabled by the emergence of strained-layer Si and SiGe epitaxy, including strained Si CMOS. <u>This course is intended for graduate students in both the Microsystems and Electronic Design and applications (EDA) TIGs, as well as any other students interested in novel microelectronics device and circuit technologies and the future of electronics.</u>

Course Outline

- Introduction
- Epitaxial SiGe Alloys
- The SiGe Heterojunction Bipolar Transistor
- Circuit Design with SiGe HBTs
- Other SiGe Heterostructure Devices
- Future Directions

Sign up Now!

Limited Space Available!



About the Prof: Cressler was awarded the 2010 Class of 1940 W. Howard Ector Outstanding Teacher Award (Georgia Tech's top teaching award), and the 2013 Class of 1934 Distinguished Professor Award (the highest honor Georgia Tech bestows on its faculty). Visit: *http://users.ece.gatech.edu/~cressler* *and* *http://johndcressler.com*

Course Syllabus

ECE 6444 “Silicon-Based Heterostructure Devices and Circuits”

School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. John D. Cressler

Chapter	Topics	Assigned Reading (C x.x = Cressler’s book section)
Chapter 0	**Getting Up to Speed**	handouts
	0.1 reminders on semiconductor physics	
	0.2 BJTs vs FETs	
	0.3 the ideal BJT	
	0.4 the non-ideal BJT	
	0.5 the generalized Moll-Ross relations	
Chapter 1	**Motivation and Overview of the Field**	
	1.1 the virtues of Si	C 1.1
	1.2 the fundamental driving forces	C 1.2-1.3
	1.3 the SiGe HBT	C 1.4-1.5
	1.4 some history	C 1.6
	1.5 trends and competitive pressures	C 1.7-1.8
	1.6 future directions	C 1.7-1.8
Chapter 2	**SiGe Strained Layer Epitaxy**	
	2.1 SiGe alloys	C 2.1-2.2
	2.2 stability issues	C 2.3
	2.3 band structure	C 2.4
	2.4 transport properties	C 2.5
Chapter 3	**SiGe HBT BiCMOS Technology**	
	3.1 fabricating SiGe HBTs	C 3.1-3.2
	3.2 carbon doping	C 3.3
	3.3 passives	C 3.4
Chapter 4	**dc and ac Characteristics of SiGe HBTs**	
	4.1 an intuitive picture	C 4.1
	4.2 collector current and current gain	C 4.2
	4.3 output conductance	C 4.3
	4.4 breakdown voltages	C 4.5-4.6
	4.5 transit times	C 5.6
Chapter 5	**Second Order Effects**	
	5.1 Ge Grading issues	C 6.1
	5.2 neutral base recombination	C 6.2
	5.3 barrier effects	C 6.3
Chapter 6	**Noise and Linearity**	
	6.1 fundamental considerations	C 7.1
	6.2 broadband noise	C 7.2-7.3
	6.3 low-frequency noise	C 7.6
	6.4 profile design tradeoffs in noise	C 7.5
	6.5 linearity issues	C 8.1-8.3
Chapter 7	**Other Topics** (time permitting)	
	7.1 temperature effects	C 9.1-9.6
	7.2 radiation effects	C 11.1-11.5
	7.3 strained-Si CMOS	handouts
	7.5 other types of Si-based devices	handouts